

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicant(s): ABE et al.	Atty. Dkt.: 01-474
Serial No.: Unknown	Group Art Unit:
Filed: Concurrently herewith	Examiner:
Title: DIODE AND PRODUCING METHOD THEREOF	

Commissioner for Patents
Arlington, VA 22202

Date: July 28, 2003

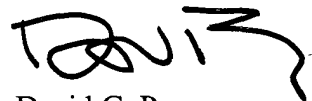
INFORMATION DISCLOSURE STATEMENT

Sir:

Pursuant to 37 C.F.R. §1.56, the reference(s) listed on the attached Form PTO-1449 is/are being submitted for consideration by the Examiner without any admission that it/they constitute(s) statutory prior art, or without any admission that it/they contain(s) subject matter that anticipates the invention or renders the invention obvious to a person of ordinary skill in the art.

The Examiner is requested to initial the attached PTO Form-1449 and to return a copy of same to the undersigned attorney as proof that the listed reference(s) has/have been considered and made of record.

Respectfully submitted,



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FORM PTO-1449	ATTY. DKT NO.	01-474	SER. NO.
	APPLICANT	ABE et al.	
	FILING DATE	July 28, 2003	GROUP

REFERENCE DESIGNATION

U.S. PATENT DOCUMENTS

EXAMINER INITIAL		DOCUMENT NUMBER	DATE	NAME	CLASS	SUB CLASS
		6,518,604	Feb. 11, 2003	Worley et al.		

FOREIGN PATENT DOCUMENTS

								TRANSLATION	
		DOCUMENT NUMBER	DATE	COUNTRY	NAME	CLASS	SUB CLASS	YES	NO
		EP 0,345,432	12/13/89	Europe				X	

* Full English text of the JP Document will be available in machine-translated form from JP (Japanese Patent Office) English language web site at <http://www1.ipdl.jpo.go.jp/PA1/cgi-bin/PA1INDEX>.

OTHER REFERENCES (including Author, Title, Date, Pertinent Pages, etc.)

		Kenji Kono, ESD surge simulation of IC for automobile, Technical Report of IEICE, SDM2002-184, Vol. 102, No 347, October 1, 2002, pp31-36
EXAMINER		DATE CONSIDERED